IEEE中華民國分會補助各支會活動成果報告表

96.5.3

會議名稱：<兩場專題演講> 1. Pushing CMOS to the Limits 2. Sub-1mW/Gbps High-Speed Links and Design Techniques Enabling Low-Power, Multi-Gigasample/s ADCs		
舉辦日期：98/4/27-98/4/28，98/4/30-98/5/1		
主辦機構：台大聯發科實驗室	舉辦地點：交通大學，台灣大學	
舉辦支會：SSC37	支會主席：陳巍仁	TEL：03-5712121*54172

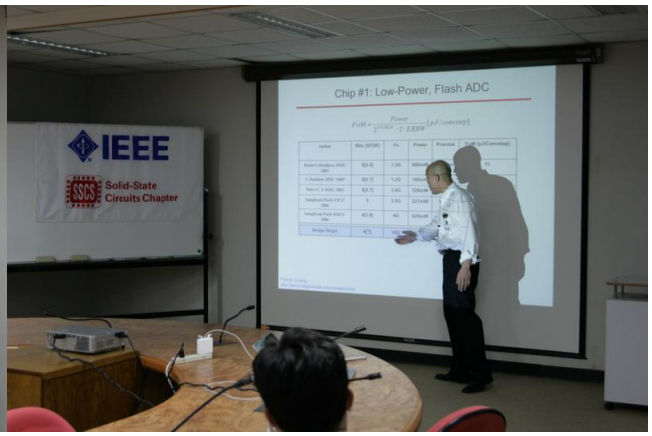
原預估出席人數：
1. Pushing CMOS to the Limits: 200 人
2. Sub-1mW/Gbps High-Speed Links and Design Techniques Enabling Low-Power, Multi-Gigasample/s ADCs: 60 人。

會議當天實際出席人數：
1. Pushing CMOS to the Limits: 236 人
2. Sub-1mW/Gbps High-Speed Links and Design Techniques Enabling Low-Power, Multi-Gigasample/s ADCs: 59 人。

會議重要成果：（請確實填寫，作為下屆補助經費參考）

請列舉本會議重要成果（含對IEEE之重要貢獻）

此專題演講邀請國外專家學者介紹無線通訊積體電路、串列傳輸積體電路+ADC，
藉以提昇國內相關技術人才設計能力，促進國內產、學界保持與國際先進技術接觸。



需繳交資料：	1. 活動文章（約500字，MS-Word格式，中英文版各乙篇） 2. 照片2-4張（JPEG檔/300dpi） ※ 上述資料請自行登錄於分會網頁，並將電子檔e-mail至陳虹妙(nao@cc.nctu.edu.tw)信箱。

1.Pushing CMOS to the Limits
主講人：Prof. Ali M. Niknejad
Associate Professor, Electrical Engineering and Computer Sciences, UC Berkeley
<第一場>
98/4/27(一) 16:30~17:30, 國立台灣大學明達館 231 室
<第二場>
98/4/28(二) 15:30~16:30, 國立交通大學工四館 528 室

主辦單位：台大-聯發無線研究實驗室
協辦單位：晶片系統國家型科技計畫辦公室，IEEE SSCS Taipei Chapter，台灣大學電子所，交通大學電子系

演講大綱
Silicon CMOS technology scaling has resulted in fast, tiny, and cheap transistors which are used as building blocks in digital, analog, and increasingly RF and video electronic devices. As the scaling continues, will the performance of analog/RF integrated circuits continue to suffer due to dynamic range limitations? Are there new opportunities or new design paradigms that can be used to overcome the limitations of CMOS? The first part of the talk will review some technological limitations related to noise, distortion, dynamic range, and speed. Performance limitations from a device and technology perspective account for only part of the story. The second part of the talk will highlight circuit design examples that overcome these limitations, allowing operation at record speeds over 100 GHz, relatively high power levels, and high linearity despite using low supply voltages and "digital" transistor technology.

2. Sub-1mW/Gbps High-Speed Links and Design Techniques Enabling Low-Power, Multi-Gigasample/s ADCs
主講人:Prof. Patrick Chiang, Oregon State University
<第一場>
98/4/30(星期四) 15:00-16:30 交通大學工四館 528 會議室
<第二場>
98/5/01(星期五) 10:30-12:00 台灣大學電機二館 105 視聽教室

主辦單位 : 台大-聯發無線研究實驗室
協辦單位 : 台大電子所，交大電子所，IEEE SSCS Taipei Chapter

演講大綱
High-speed serial links are limited by two major constraints: 1) power consumption, in regards to energy/bit transmitted; 2) limited bandwidth due to channel losses. In this talk, I will show recent design techniques we have used at the VLSI group at Oregon State in order to tackle these two issues.
First, I will discuss the design of low-power, highly parallel serial links, and the analysis of low-power clock generation/distribution to many of these links. I will also show preliminary measurements of distributed injection-locked ring oscillators in 90nm-CMOS for clock distribution, enabling 0.6mW/Gbps, 7-8Gbps serial link receivers for short-range interconnects.
Second, I will discuss the design of multi-gigahertz sample rate ADCs (i.e. 10+ GSs, 6b, 100mW), used for many applications such as mm-wave RF systems and band-limited serial links. I will show measurement results of time-interleaved phase calibration for an 8 gigasample/s ADC in 90nm-CMOS, showing residual phase offset after statistical averaging reduced from 22ps to < 1ps.